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INSULATED GATE TYPE FIELD SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF (English)
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JP 2000294797	A2	20001020	JP 200068187	A	19901225	
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JP 2791422	B2	19980827	JP 90418366	A	19901225	
JP 2997737	B2	20000111	JP 90418367	A	19901225	
JP 3029289	B2	20000404	JP 90316598	A	19901120	
JP 3362022	B2	20030107	JP 200068187	A	19901225	
KR 9513784	B1	19951116	KR 9120771	A	19911120	
US 5453858	A	19950926	US 384593	A	19950203	
US 5514879	A	19960507	US 479392	A	19950607	
US 5614732	A	19970325	US 293201	A	19940819	
US 5701167	A	19971223	US 712574	A	19960913	
US 5849601	A	19981215	US 231644	A	19940422	
US 5859445	A	19990112	US 799369	A	19970214	
US 6011277	A	20000104	US 149290	A	19980909	
US 6023075	A	20000208	US 962601	A	19971031	
US 20010014535	AA	20010816	US 832844	A	20010412	
US 20010054714	AA	20011227	US 901026	A	20010710	
US 6252249	BA	20010626	US 854037	A	19970509	
US 6281520	BA	20010828	US 149291	A	19980909	
US 6306213	BA	20011023	US 962600	A	19971031	

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JP 90316598 A 19901120
JP 90323696 A 19901126
JP 90418366 A 19901225
JP 90418367 A 19901225
JP 200068187 A 19901225
US 384593 A 19950203
US 217211 B1 19940324
US 811063 B1 19911220
US 479392 A 19950607
US 293201 A3 19940819
US 967564 B1 19921028

US 673821 B1 19910322
US 293201 A 19940819
US 712574 A 19960913
US 500241 B1 19950710
US 384593 A3 19950203
US 231644 A 19940422
US 217211 B3 19940324
US 799369 A 19970214
US 149290 A 19980909
US 799369 A3 19970214
US 962601 A 19971031
US 231644 A3 19940422
US 293201 A2 19940819
US 832844 A 20010412
US 962600 A3 19971031
US 293201 A1 19940819
US 901026 A 20010710
US 149291 A3 19980909
US 854037 A 19970509
US 673821 A1 19910322
US 149291 A 19980909
US 962600 A 19971031
US 811063 A1 19911220

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(54)[TITLE OF THE INVENTION] LIQUID CRYSTAL DISPLAY DEVICE

(57)[Abstract]

[PURPOSE] The present invention aims at providing a liquid crystal display device at an increased production yield with a reduced production cost.

[CONSTITUTION] A liquid crystal display device comprising a first substrate having provided thereon a pixel matrix comprising a plurality of gate lines and a plurality of source (drain) lines and a thin film transistor and a second substrate opposed to the first substrate, and a liquid crystal composition having sandwiched therebetween, wherein at least one part of said peripheral circuits being connected to the matrix wirings in X-direction or Y-direction formed on the first substrate has a complementary structure with active elements to form thin film transistors fabricated by the same process, and the remaining parts of the peripheral circuits are constructed from semiconductor chips.

[WHAT IS CLAIMED IS:]

1. A liquid crystal display device comprising:

a first substrate having provided thereon a pixel matrix comprising a plurality of gate lines and a plurality of source (drain) lines and a thin film transistor established in complementary structure;

a second substrate opposed to the first substrate; and

a liquid crystal composition having sandwiched between the first substrate and the second substrate, wherein, among the peripheral circuits being connected to the matrix wirings in X-direction or Y-direction formed on the first substrate, at least one part of said peripheral

circuits is constructed from thin film semiconductor devices fabricated in complementary structure by the same process utilized for the thin film transistors, and the remaining halves of the peripheral circuits are constructed from semiconductor chips.

2. The liquid crystal display device of claim 1 wherein the peripheral circuits constructed from semiconductor chips is connected to the matrix wirings by COG method.

3. The liquid crystal display device of claim 1 wherein the thin film transistor is constructed from semi-amorphous semiconductor.

[DETAILED DESCRIPTION OF THE INVENTION]

[0001]

[FIELD OF THE INVENTION]

The present invention relates to a liquid crystal display device formed by using thin film transistors.

[0002]

[DESCRIPTION OF PRIOR ART]

More attention is paid to flat displays than to CRTs for use in office automation (OA) machines and the like, and particularly, there is an increasing demand for large-area display devices. Also, as other application of flat displays, wall television (TV) is developed at a fast speed. Furthermore, there are demands for color flat displays and finer display images.

[0003]

A liquid crystal display device is known as a representative example of the flat displays. The liquid crystal display device comprises a liquid crystal composition having an electrode interposed between a pair of glass substrates, and the images are displayed by the change of state of the liquid crystal composition upon application of an electric field thereto. The liquid crystal may be driven by the use of a thin film transistor (referred to hereinafter as a TFT) or other switching elements, or by making it into a simple matrix structure. In any case, a driver circuit is established at the periphery of a display to supply signals for driving liquid crystals to column and row directions (X, Y).

[0004]

The driver circuit is generally composed of MOS integrated circuit (IC) made of a single crystal silicon. The IC is provided with pad electrodes

corresponding to each of the display electrodes, and a printed substrate is incorporated between the pad and the display electrodes to connect first the pad electrode of the IC with the printed substrate and then the printed substrate with the display. The printed substrate is made of an insulator substrate such as a glass epoxy or a paper filled epoxy, or of a flexible plastic substrate. It requires an area equivalent to or even larger than the display area. Similarly, the volume thereof should have to be made considerably large.

[0005]

[PROBLEMS TO BE SOLVED BY THE INVENTION]

Thus, because of the construction as described hereinabove, a conventional display has defects as follows.

[0006]

Namely, (1) a superfine display cannot be realized since the same number of the display electrodes for the X direction and the Y direction of the matrix wirings, or the source (drain) wirings, or the gate wirings should be connected to the printed substrate, and the distance between the connecting portions technologically achievable by the up-to-date surface mounting technology is limited to a certain length.

[0007]

(2) A display device needs the printed substrate, the ICs, and the connecting wirings in addition to the display itself, which require an area and volume about several times as large as those of the display itself.

[0008]

(3) The connections are of low reliability since quite a large number of connections should be established between the main display and the printed substrate, as well as between the printed substrate and the ICs; moreover, not a small weight is casted on the connecting portions.

[0009]

As a means to overcome the foregoing defects, there is a proposal that a display device, particularly a display using active elements as the switching element construct the active element and the peripheral circuits on a same substrate using TFTs. Such a construction indeed solves the three problems mentioned hereinabove, however, it newly develops problems as follows.

[0010]

(4) Since the peripheral circuits as well as an active element also are made from TFTs, the number of the elements to be fabricated on the same substrate is increased and hence the production yield of the TFT is lowered. Therefore, the production yield of the display is decreased.

[0011]

(5) The peripheral circuit portion comprises a very complicated element structure as compared with the element structure at a portion of active elements. Therefore, circuit patterns are complicated and the technique of manufacturing processes became high-level, thereby the production cost is increased. Furthermore, with the increase in the multilayered wiring portion, an increase in process steps as well as a decrease in the production yield of the TFTs occur.

[0012]

(6) Since a quick response is required to the transistors which constitute the peripheral circuit, a polycrystalline semiconductor is generally used. Therefore, it requires a treatment at a high temperature and hence an expensive quartz substrate should be used to obtain a polycrystalline semiconductor layer.

[0013]

[CONSTITUENTS OF THE INVENTION]

The present invention solves the six problems mentioned above by taking balance among them and provides a low-priced liquid crystal display device at a high production yield.

[0014]

Namely, the present invention have been attained by a liquid crystal display device comprising a first substrate having provided thereon a pixel matrix comprising a plurality of gate lines and a plurality of source (drain) lines and a thin film transistor established in a complementary structure and a second substrate opposed to the first substrate, and a liquid crystal composition having sandwiched therebetween, wherein, among the peripheral circuits being connected to the matrix wirings in X-direction or Y-direction, at least one part of said peripheral circuits is established in complementary structure by the same process utilized for the active element connected to the pixel, and the rest of the peripheral circuits are constructed from semiconductor chips.

[0015]

The ICs of the residual peripheral circuits which are not fabricated as TFTs are connected with the substrate by a COG process which comprises directly mounting the IC chips on a substrate and connecting them with each of the connecting terminals, and a TAB process which comprises mounting each of the IC chips on a flexible substrate made of an organic resin, and then connecting the resin substrate with the display substrate.

[0016]

According to the present invention, all of the peripheral circuits are not fabricated as TFTs. In stead of this, only a part having simple element structure, or only a functional portion having a small number of elements, or only a circuit portion which is difficult portion of a general use ICs, or only a portion which has expensive ICs is fabricated as TFTs, thereby production yields of liquid crystal display devices are improved and the production cost are reduced.

[0017]

Also, one part of peripheral circuits is fabricated as TFTs, the manufacturing cost is reduced by decreasing the number of external Ics. Conventionally, quite large number of the external Ics have been required.

[0018]

Further, since the thin film transistor has a complementary structure (CTFT) wherein active elements and the peripheral circuits are fabricated by the same process, the ability of driving the pixels is improved and the peripheral circuits has redundancy, thereby it is possible to drive the liquid crystal display device.

[0019]

If the peripheral circuits were to be wholly fabricated into TFTs, the device requires extension of the display substrate along both of the X and Y directions. This leads to an increase in the total occupancy area of the display device itself. In contrast, if only one part of the peripheral circuits were to be fabricated into TFTs, it results a little extension of the substrate which can be readily accommodated to the outer dimension of the computers and other apparatuses to which the display device is assembled. Thus, there is provided a display device having a small occupancy area and volume.

[0020]

A high-leveled technique is required to fabricate the complicated portions of element structure in the peripheral circuit, for example, a element structure which requires a multilayered wiring, or a portion having a function as an amplifier. However, by fabricating one part into TFTs, the conventional ICs are used in a portion where high technique is required and simple element structure or portions of simple function can be made with TFTs. As a result, a display device can be realized at reduced cost with a high yield.

[0021]

Furthermore, by fabricating only one part into TFTs, the number of the TFTs in the peripheral circuit portion can be considerably reduced. For example, the number of the TFTs can be almost halved in the case that the

peripheral circuits for the X and the Y directions have the same function. In this way, it is possible, by reducing the number of elements to be fabricated as TFTs, to increase the production yield of the substrate. In addition, there is provided a low cost display device reduced both in the area of the substrate and in volume.

[0022]

It is further possible to fabricate the semiconductor layers of the TFTs at a lower temperature and yet to realize quick response TFTs having a considerably increased carrier mobility by using semi-amorphous semiconductor according to a new concept , instead of the conventional polycrystalline or amorphous semiconductors used for TFTs,.

[0023]

The semi-amorphous semiconductor can be obtained by applying a heat treatment to crystallize a thin film having deposited by processes such as low-pressure chemical vapor deposition (LPCVD), sputtering, plasma-assisted chemical vapor deposition (PCVD), and the like. The process for fabricating a semi-amorphous semiconductor film is described below referring to the sputtering process as an example.

[0024]

Namely, sputtering is performed by using a single crystal silicon semiconductor as a target under a mixed gas comprising hydrogen and argon. Then, the heavy argon atoms strike the surface of the silicon target, thereby silicon atoms are released from the target and then travel to the substrate on which the film is to be deposited, accompanied by clusters composed of several tens to several millions of silicon atoms.

[0025]

During their travel, hydrogen atoms come to bond with the dangling bonds of the silicon atoms located at the outer periphery of the clusters, and these clusters comprising the silicon-hydrogen bonding are maintained to the surface of the substrate to deposit as a relatively ordered region. Thus, a highly ordered film comprising a mixture of pure amorphous silicon and clusters accompanied by Si-H bondings on the periphery is realized on the surface of the substrate. By further heat treatment of the deposited film at the temperature range of from 450 to 700°C in a non-oxidizing atmosphere, the Si-H bondings on the outer periphery of the clusters react with each other to yield Si-Si bondings.

[0026]

The Si-Si bondings thus obtained exert a strong attractive force to each other. At the same time, however, the clusters in their highly ordered state

are susceptible to undergo phase transition to attain a more ordered state, i.e., a crystallized state. Thus, because the Si-Si bondings in the neighboring clusters attract each other, the resulting crystals suffer lattice distortion which can be observed by laser Raman spectroscopy as a peak deviated in position to the lower frequency side from the 520cm^{-1} which corresponds to the peak of a single crystal of silicon.

[0027]

Furthermore, since the Si-Si bondings between the neighboring clusters cause anchoring (connecting) effects, the energy band in each cluster is electrically connected with that of the neighboring cluster through the anchored locations. Accordingly, since there is no grain boundaries as in the conventional polycrystalline silicon which function as a barrier to the carriers, a carrier mobility as high as in the range of from 10 to 200cm^2/V.sec can be obtained.

[0028]

That is, the semi-amorphous semiconductor defined above has apparently crystallinity, however, if viewed from the electrical properties, there can be assumed a state substantially free from grain boundaries. If the annealing of a silicon semiconductor were to be effected at a temperature as high as 1000°C or over, instead of a moderate annealing in the temperature range of from 450 to 700°C as referred hereinbefore, the crystallization naturally would induce crystal growth to precipitate oxygen and the like at the grain boundaries and would develop a barrier. The resulting material is then a polycrystalline material comprising single crystals and grain boundaries.

[0029]

In the semi-amorphous semiconductors, the carrier mobility increases with elevating degree of anchoring. To enhance the carrier mobility, the oxygen content of the film should be controlled to 7 X 10^{19} cm^{-3} or lower, preferably, to 1 X 10^{19} cm^{-3} or lower, thereby the crystallization can be taken place at a temperature lower than 600°C and high carrier mobility can be obtained.

[0030]

[EXAMPLE 1]

In the present example, a liquid crystal display device having an m X n circuit structure shown in FIG. 1 is described. Namely, among peripheral circuits being connected to a wiring of the X-direction shown in Fig. 1, only analog switch alley circuit portion 1 is fabricated as TFTs 5 in a similar manner as an active element provided to a pixel 6. Also, only analog switch

array portion 2 in the peripheral portion connected to wirings in Y-direction is fabricated in TFTs and the residual peripheral circuit portions connected to substrates as IC4 by COG method. According to the present invention, the peripheral circuit portion fabricated as TFTs is formed as a CTFT in a similar manner as an active element provided in pixels.

[0031]

The actual arrangement of the electrodes and the like corresponding to this circuit structure is shown in FIG. 2. In FIG. 2, however, the structure is simplified and shown in a 2 X 2 structure.

[0032]

Referring to FIG. 3, the process for fabricating the TFTs of the liquid crystal display device according to the present invention is firstly explained. In FIG. 3(A), a silicon oxide film is deposited to a thickness of from 1,000 to 3,000Å as a blocking layer 51 by magnetron radio frequency (RF) sputtering on a glass substrate 50 made of an economical glass such as a quartz glass which resists to heat treatment performed at a temperature of 700°C or less, e.g., about 600°C. The actual film deposition was carried out in a 100% oxygen atmosphere at a film deposition temperature of 15°C, at an output of from 400 to 800W, and a pressure of 0.5 Pa. The film deposition rate using a quartz or a single crystal silicon as the target was in the range of from 30 to 100Å/minute.

[0033]

On the silicon oxide film thus obtained was further deposited a silicon film by LPCVD (low-pressure chemical vapor deposition), sputtering, or plasma-assisted CVD (PCVD). In the case of using the LPCVD process, film deposition was conducted at a temperature lower than the crystallization temperature by 100 to 200°C, i.e., in the range of from 450 to 550°C, e.g., at 530°C, by supplying disilane (Si_2H_6) or trisilane (Si_3H_8) to the CVD apparatus. The pressure inside the reaction chamber was controlled to be in the range of from 30 to 300 Pa. The film deposition rate was 50 to 250Å/minute. Furthermore, optionally boron may be supplied to 1×10^{15} to 1×10^{18} cm^{-3} in the film as diborane during the film deposition to control the threshold voltage (Vth) of the N-TFT and that of the P-TFT to be approximately the same.

[0034]

In the case of using sputtering, the back pressure prior to sputtering was controlled to 1×10^{-5} Pa or lower and film deposition was conducted using a single crystal silicon as the target in an atmosphere having an argon added with hydrogen of 20 to 80%. For example, the atmosphere contains

20% of argon and 80% of hydrogen. The film was deposited at a film deposition temperature of 150°C, a frequency of 13.56 MHz, a sputter output of from 400 to 800W, and a pressure of 0.5 Pa.

[0035]

In the case of depositing a silicon film by a plasma CVD process, the temperature was maintained, e.g., at 300°C, and monosilane (SiH_4) or disilane (Si_2H_6) was used. A high frequency electric power was applied at 13.56 MHz to the gas inside the PCVD apparatus to effect the film deposition.

[0036]

The films thus obtained by the foregoing processes preferably contain oxygen at a concentration of 5×10^{21} cm^{-3} or lower. If the oxygen concentration is too high, the film thus obtained would not crystallize. Accordingly, there would be required to elevate the thermal annealing temperature or to take a longer time for the thermal annealing. Too low an oxygen concentration, on the other hand, increases an off-state leak current due to a backlighting. Accordingly, the preferred range of the oxygen concentration was set in the range of from 4×10^{19} to 4×10^{21} cm^{-3}. The hydrogen concentration was for example 4×10^{20} cm^{-3}, which accounts for 1% by atomic with respect to the silicon concentration of 4×10^{22} atoms.cm^{-3} To enhance crystallization of the source and drain portions, oxygen concentration is 7×10^{19} cm^{-3} or less, preferably 1×10^{19} cm^{-3} or less and oxygen may be added selectively by ion-implantation to the channel forming regions of the TFT which constitute the pixel, to such an amount to give a concentration in the range of from 5×10^{20} to 5×10^{21} cm^{-3}. Since no light was irradiated to the TFTs in the peripheral circuit, it was effective to impart thereto a higher carrier mobility while reducing the oxygen concentration in order to realize a high frequency operation.

[0037]

After the amorphous silicon film was deposited at a thickness of from 500 to 5,000Å, e.g., at a thickness of 1,500Å, the amorphous silicon film was then heat-treated at a moderate temperature in the range of from 450 to 700°C for a duration of from 12 to 70 hours in a non-oxidizing atmosphere. More specifically, the film was maintained at 600°C under a hydrogen atmosphere. Since on the surface of the substrate was provided an amorphous silicon oxide layer under the silicon film, the whole structure was uniformly annealed because there was no nucleus present during the heat treatment. That is, during the film deposition step, the film construction maintains the amorphous structure and the hydrogen is present as a mixture.

[0038]

The silicon film then undergoes phase transition from the amorphous structure to a structure having a higher degree of ordering by the annealing, and partly develops a crystallized portion. Particularly, the region which attains a relatively high degree of ordering at the film deposition of silicon tend to crystallize at this stage. However, the silicon bonding which bonds the silicon atoms each other attracts a region to another. This effect can be observed by a laser Raman spectroscopy as a peak shifted to a lower frequency side as compared with the peak at $522cm^{-1}$ for a single crystal silicon. The apparent grain size can be calculated by the half width as 50 to 500Å, i.e., a size corresponding to that of a microcrystal, but in fact, the film has a semi-amorphous structure comprising a plurality of those highly crystalline regions yielding a cluster structure, and the clusters are anchored to each other by the bonding between the silicon atoms.

[0039]

As a result, the film yields a state in which no grain boundary (referred to hereinafter as GB) exists. Since the carrier easily moves between the clusters via the anchoring, a carrier mobility far higher than that of a polycrystalline silicon having a distinct GB can be realized. More specifically, a hole mobility(μh) in the range of from 10 to $200cm^2/Vsec$ and an electron mobility (μe) in the range of from 15 to $300cm^2/Vsec$ are achieved.

[0040]

On the other hand, if a high temperature annealing in the temperature range of from 900 to 1200°C were to be applied in the place of a moderate temperature annealing as described hereinabove, impurities undergo a solid phase growth from the nuclei and segregate in the film. This results in the high concentration of oxygen, carbon, nitrogen, and other impurities at the GB into a barrier. Thus, despite the high mobility within a single crystal, the carrier is interfered at its transfer from a crystal to another by the barrier at the GB. In practice, it is quite difficult to attain a mobility higher than or equal to $10cm^2/Vsec$ with a polycrystalline silicon at the present. Thus, in the example, a semi-amorphous or a semi-crystalline structured silicon semiconductor is utilized.

[0041]

Referring to FIG. 3(A), the silicon film was masked with a first photomask <l>, and subjected to photo-etching to obtain the region 22 (having a channel width of 20μm) for the P-TFT on the right-hand side of the FIGURE and the region 13 for the N-TFT on the left-hand side of the FIGURE.

[0042]

On the resulting structure was deposited a silicon oxide film as the gate insulating film to a thickness of from 500 to 2,000Å, e.g., 1,000Å. The conditions of the film deposition were the same as those employed in depositing the silicon oxide film as a blocking layer. Alternatively, a small amount of fluorine may be added during the film deposition to fix sodium ions.

[0043]

Further on the gate insulating film was deposited a silicon film doped with phosphorus at a concentration of from 1×10^{21} to 5×10^{21} cm^{-3}, or a multilayered film composed of said silicon film doped with phosphorus, having provided thereon a layer of molybdenum (Mo), tungsten (W), $MoSi_2$, or WSi_2. The resulting film was patterned using a second photomask <2> to obtain a structure as shown in FIG. 3(B). Then, a gate electrode 55 for the P-TFT, and a gate electrode 56 for the NTFT were established, for example, by depositing first a 0.2μm thick phosphorus(P)-doped silicon and a 0.3μm thick molybdenum layer thereon, at a channel length of 10μm. Referring to FIG. 3(C), a photoresist 57 was provided using a photomask <3>, and to a source 59 and a drain 58 for the P-TFT were added boron by ion implantation at a dose of from 1×10^{15} to 5×10^{15} cm^{-2}. Then, as shown in FIG. 3(D), a photoresist 61 was provided using a photomask <4>, and to a source 64 and a drain 62 for the N-TFT was added phosphorus by ion implantation at a dose of from 1×10^{15} to $5 \times 10^{15} cm^{-2}$.

[0044]

The processes above were carried out via a gate insulating film 54. However, referring to FIG. 3(B), the silicon oxide on the silicon film may be removed utilizing the gate electrodes 55 and 56 as the masks, and then boron and phosphorus may be directly added to the silicon film by ion implantation.

[0045]

The structure thus obtained was re-annealed by heating at 600°C for a duration of from 10 to 50 hours. The impurities in the source 59 and drain 58 of the P-TFT and those in the source 64 and drain 62 of the N-TFT were activated to obtain P+ and N+ TFTs. Under the gate electrodes 55 and 56 were provided channel forming regions 60 and 63 with a semi-amorphous semiconductor.

[0046]

According to the process, a CTFT can be obtained in a self-aligned method without elevating the temperature to 700°C or higher. Thus, there is no need to use a substrate made of an expensive material such as quartz, and

therefore it can be seen that the process is suited for fabricating liquid crystal display devices of large pixels according to the present invention.

[0047]

The thermal annealing in this example was conducted twice, i.e., in the steps of fabricating the structures shown in FIGS. 3(A) and 3(D). However, the annealing at the step illustrated in FIG. 3(A) may be omitted depending on the desired characteristics, and the annealing at the step shown in FIG. 3(D) can cover the total annealing. In this way it is possible to speed up the fabrication process. Referring to FIG. 3(E), a silicon oxide film was deposited as an interlayer insulator 65 by the sputtering process mentioned hereinbefore. The method of depositing the silicon oxide film is not restricted to a sputtering method, and there may be employed LPCVD, photo CVD, or normal pressure CVD. The silicon oxide film was deposited, e.g., to a thickness of from 0.2 to 0.6μm, and an opening 66 for the electrode is formed by using a photomask <5>. The structure was then wholly covered with aluminum by sputtering, and after providing lead portions 71 and 72, as well as contacts 67 and 68 using a photomask <6>, the surface thereof was coated with a smoothing film of an organic resin 69 such as a transparent polyimide resin, and subjected again to perforation for the electrodes using a photomask <7>.

[0048]

As shown in FIG. 3(F), two TFTs were established in a complementary structure. To the output terminal thereof was provided an Indium Tin Oxide (ITO) film by sputtering to thereby connect the TFTs with one of the transparent pixel electrodes of the liquid crystal display device. In this case, the ITO film was deposited in the temperature range from room temperature to 150°C, and then finished by annealing in oxygen or in atmosphere in the temperature range of from 200 to 400°C. The ITO film was then etched using a photomask <8> to form an electrode 70. Thus was finally obtained a structure comprising a P-TFT 22, an N-TFT 13, and an electrode 70 made of a transparent conductive film on a single glass substrate 50. The resulting TFT yielded a mobility of 20 (cm^2/Vs) and a Vth of -5.9 V for the P-TFT, and a mobility of 40(cm^2/Vs) and a Vth of 5.0 V for the N-TFT.

[0049]

Referring to FIG. 2, the arrangement of electrodes and the like in the pixel portion of the liquid crystal display device is explained. An N-TFT 13 is assembled at the crossing of a first scanning line 15 and a data line 21, and another pixel N-TFT is provided at the crossing of the first scanning line 15 with another data line 14. On the other hand, a P-TFT is assembled at the

crossing of a second scanning line 18 and a data line 21. Further, to the neighboring crossing of another first scanning line 16 and the data line 21 is provided another pixel N-TFT. Thus is accomplished a matrix structure using CTFTs. The N-TFT 13 is connected to the first scanning line 15 via a contact at the input terminal of the drain portion 64, and the gate portion 56 is connected to the data line 21 established in a multilayered wiring structure. The output terminal of the source portion 62 is connected to the pixel electrode 17 via a contact.

[0050]

The P-TFT 22, on the other hand, is connected to the second scanning line 18 by the input terminal of the drain portion 58 via a contact, while the gate portion 55 is connected to the data line 21, and the output terminal of the source portion 59 is connected to the pixel electrode 17 via a contact in the same manner as in the N-TFT. In this manner, a single pixel is established between (inner side) a pair of scanning lines 15 and 18, with a pixel 23 comprising a transparent conductive film and a CTFT. By extending this basic pixel structure in four directions, a 2 X 2 matrix can be scaled up to give a large pixel liquid crystal display device comprising a 640 X 480 or a 1280 X 960 matrix.

[0051]

It can be seen therefrom that the peripheral circuit is provided as a CMOS structure comprising an N-TFT 13 and a P-TFT 22 both fabricated in the same process as that employed for the switching element.

[0052]

As mentioned above, the substrate was laminated with the facing substrate by a known process, and an STN (super-twisted nematic) liquid crystal was injected between the substrates. The ICs 4 were used for the residual peripheral circuit. The ICs 4 were connected with each of the wirings for the X direction or Y direction on the substrate by a COG process. The ICs 4 are respectively connected to power source and connection lead for supplying data, however, all of one surface substrate is not covered with EPC for connection. Therefore, the number of the connecting portion is considerably decreased and the reliability is improved. As mentioned above, the liquid crystal display device according to the present invention is completed.

[0053]

In the embodiment, only analog switching array portion 1 among the peripheral circuits at the side of the X-direction was fabricated as TFTs and only analog switching array portion 2 among the peripheral circuits at the the

side of the Y-direction was fabricated as TFTs. C/TFT is fabricated in a similar process as a switching element while the rest of the peripheral circuits are constructed as ICs 4. The present invention, however, is not only limited to this construction, and the portion which can be more easily fabricated into TFTs can be selected depending on the yield and the problems related to the process technology at the fabrication of the TFTs.

[0054]

As described above, semi-amorphous semiconductor was used as a semiconductor film and it yields a mobility ten times as high as, or even higher than that of the TFT using a conventional non-single crystal semiconductor. Thus, it can be applicable for the TFT in the peripheral circuits in which a rapid response is required, without subjecting the TFTs in the peripheral circuit portion to a special crystallization treatment which was requisite in the conventional TFTs; as a result, the TFTs for the peripheral circuit portion could be fabricated by the same process utilized for fabricating an active element.

[0055]

Also, since an active element connected to the pixels in a liquid crystal is fabricated in C/TFT structure, the operational margin is increased and the electric potential of pixels is stable to keep a certain display level. Also, if one of TFTs is defective, it has an advantage that there is no remarkable defect in display.

[0056]

[EXAMPLE 2]

In FIG. 4 is given a schematic view of a liquid crystal display device according to another embodiment of the present invention. The basic circuits and the like are the same as those employed in the liquid crystal display device described in Example 1. Referring to FIG. 4, the portions constructed with ICs 4 among the peripheral circuits connected to the wirings for the Y-direction have the IC directly provided on the substrate by a COG method.

[0057]

The pad electrodes of the ICs 4 can be connected with the wirings of the Y-direction at a narrower interval instead of the case of forming ICs at only one side. Thus, the process of the present example enables a finer display pixel design. Furthermore, since the ICs are provided on the substrate, the total volume of the display device remains almost unchanged to give a thinner liquid crystal display device.

[0058]

In the examples described above, the TFTs of the active element were

each fabricated into a CMOS structure. However, this structure is not limited to the structure but the structure with only N-TFTs or with only P-TFTs are also acceptable. In the case, however, the number of the elements in the peripheral circuit would be increased.

[0059]

Furthermore, the position at which the TFTs are established can be varied. That is, the TFT need not be provided only to one side, i.e., only to either of the sides connected to the wirings of the X direction and the Y direction, but there may be also provided a second TFT on the other side to connect the TFTs in turns to halve the TFT density. Such a structure realizes an increase in the production yield.

[0060]

[EFFECTS OF THE INVENTION]

According to the present invention, the superfine liquid crystal display devices can be realized with no limitations of the outer connection. Furthermore, the reliability on the connections is improved, since unnecessary connections between the outer peripheral circuits and the wirings along the X and Y directions are minimized.

[0061]

The area occupation of the display substrate itself is reduced, since only a part of the peripheral circuits is fabricated into a TFT. It also allows a more freely designed substrate having a shape and dimension according to the requirements. Further, it is possible to reduce the production cost, since the problems related to the production of the TFTs can be avoided while making those portions having a higher production yield into TFTs.

[0062]

The use of a semi-amorphous semiconductor as the semiconductor film of the TFTs enables a rapid response, making the TFTs well applicable to peripheral circuits. Thus, the TFTs for the peripheral circuits are readily fabricated simultaneously utilizing the fabrication process for the active elements without any additional special treatments.

[0063]

According to the present invention, TFTs in a complementary structure are connected to each of pixels in a matrix form, thereby a lot of advantages can be obtained as follows: (1) The threshold voltage is clear. (2) an increase of the switching speed (3) an increase of an operational margin (4) If there is a defective TFT, residual TFTs can compensate them to certain degree. (5) The number of photomasks required for manufacturing processes is increased by twice in comparison with the conventional example which uses

only NTFT. (6) The carrier mobility of the present invention is ten times or more as large as the case of using an amorphous silicon, so that the size of TFTs can be decreased with no decrease of an aperture ration in the case that two TFTs are established inside one pixel.

[0064]

Because of this, in contrast with conventional active TFT liquid crystal devices using only NTFT, the production yield can be improved and the display has vivid image.

[BRIEF DESCRIPTION OF DRAWINGS]

FIG. 1 is a liquid crystal display device according to the present invention, composed of an m X n circuit structure;

FIG. 2 is an appearance of arrangement of pixel portions in a liquid crystal display according to the present invention.

FIG. 3 shows an outline of manufacturing process of TFTs according to the present invention.

FIG. 4 shows other embodiment of the present invention.

[DESCRIPTION OF MARKS]

1, 2, . . . peripheral circuit

4 . . . IC

5 . . . peripheral circuit fabricated into TFT

6 . . . pixel

13 . . . NTFT

22 . . . PTFT

[Procedural Amendment]
[Date of Submission] FEBRUARY 18, 1992
[Procedural Amendment 1]
[Title of Document to be Amended] Specification
[Title of Item to be Amended] Brief description of drawings
[Method] Modification
[Content of Amendment]
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FIG. 1 is a liquid crystal display device according to the present invention, composed of an m X n circuit structure;
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[DESCRIPTION OF MARKS]
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[Procedural Amendment 2]
[Title of Document to be Amended] Drawing
[Title of Item to be Amended] all drawings
[Method] Modification
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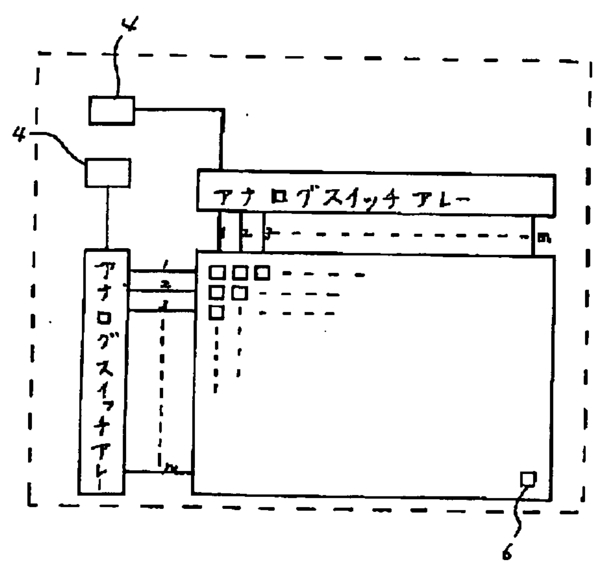
(54)【発明の名称】　液晶表示装置

(57)【要約】

【目的】　本発明はコストが低く、製造歩留りの高い液晶表示装置を提供することを目的とする。

【構成】　複数のゲート線、複数のソース（ドレイン）線および薄膜トランジスタを有する画素マトリクスが形成された第１の基板と前記第１の基板に対抗して配置された第２の基板と前記一対の基板間に保持された液晶組成物よりなる液晶表示装置であって、前記第１の基板上に形成されるＸまたはＹ方向のマトリクス配線に接続されている周辺回路のうちの少なくとも一部の周辺回路とアクティブ素子とを相補型構成として、同一のプロセスで形成された薄膜トランジスタとし、残りの周辺回路は半導体チップで構成されているものであります。



【特許請求の範囲】

【請求項１】複数のゲート線、複数のソース（ドレイン）線および相補型構成の薄膜トランジスタを有する画素マトリクスが形成された第１の基板と前記第１の基板に対抗して配置された第２の基板と前記一対の基板間に保持された液晶組成物よりなる液晶表示装置であって、前記第１の基板上に形成されるＸまたはＹ方向のマトリクス配線に接続されている周辺回路のうち少なくとも一部の周辺回路を前記画素に接続されたアクティブ素子と同様の相補型構成にて、同一のプロセスで形成された薄膜半導体装置とし、前記周辺回路のうち残りの部分は半導体チップで構成されていることを特徴とする液晶表示装置。

【請求項２】請求項１に記載の半導体チップで構成されている周辺回路はＣＯＧ法によりマトリクス配線と接続されていることを特徴とする液晶表示装置。

【請求項３】請求項１に記載の薄膜半導体装置はセミアモルファス半導体により構成されていることを特徴とする液晶表示装置。

【発明の詳細な説明】

【０００１】

【産業上の利用分野】本発明は薄膜トランジスタを用いて形成される液晶表示装置に関する。

【０００２】

【従来の技術】ＯＡ機器等のディスプレイとしてＣＲＴに代わりフラットディスプレイが注目され、特に大面積化への期待が強くなってきている。またフラットディスプレイのその他の応用として壁掛けＴＶの開発も急ピッチで進められている。また、フラットディスプレイのカラー化、高精細化の要求も相当高まってきている。

【０００３】このフラットディスプレイの代表例として液晶表示装置が知られている。これは一対のガラス基板間に電極を挟んで保持された液晶組成物に電界を加えて、液晶組成物の状態を変化させ、この状態の違いを利用して、表示を行う。この液晶の駆動のために薄膜トランジスタ（以下ＴＦＴという）やその他のスイッチング素子を設けたものや単純にマトリクス構成を持つものがある。何れの場合も、縦横（Ｘ、Ｙ）方向の各配線に対して液晶を駆動するための信号を送り出すドライバー回路がディスプレイ周辺に設けられている。

【０００４】このドライバー回路は通常は単結晶シリコンのＭＯＳ集積回路（ＩＣ）で構成されている。このＩＣには各ディスプレイ電極に対応するパッド電極が設けられており、この両者の間にプリント基板が介在し、先ずＩＣのパッド電極とプリント基板を接続し、次にプリント基板とディスプレイを接続していた。このプリント基板はガラスエポキシや紙エポキシの絶縁物基板またはフレキシブルなプラステイックよりなる基板であり、その占有面積はディスプレイと同じかまたはそれ以上の面積が必要であった。また、同様に容積も相当大きくする必要があった。

【０００５】

【発明が解決しようとする課題】このような従来のディスプレイは前述のような構成のため以下のような欠点を有していた。

【０００６】すなわち、①マトリクス配線のＸ方向、Ｙ方向の表示電極またはソース（ドレイン）配線またはゲート配線の数と同数の接続がプリント基板との間で行われるために、実装技術上接続可能な各接続部間の間隔に制限があるために、高精細な表示ディスプレイを作製することはできなかった。

【０００７】②表示ディスプレイ本体以外にプリント基板、ＩＣおよび接続配線が必要であり、その必要面積および必要容積はディスプレイ本体の数倍にも及んでいた。

【０００８】③ディスプレイ本体とプリント基板およびプリント基板とＩＣとの接続箇所が多く、しかも、かなりの重量があるので接続部分に無理な力が加わり、接続の信頼性が低かった。

【０００９】一方、このような、欠点を解決する方法として、ディスプレイ特にアクティブ素子をスイッチング素子として使用した表示装置において、アクティブ素子と周辺回路とを同じ基板上にＴＦＴで構成することが提案されている。しかしながらこの構成によると前述の３つの欠点はほぼ解決することができるが、新たに以下のような別の問題が発生した。

【００１０】④アクティブ素子以外に周辺回路をもＴＦＴ化した為に、同一基板上に形成する素子の数が増し、ＴＦＴの製造歩留りが低下した。従ってディスプレイの製造歩留りも低下した。

【００１１】⑤アクティブ素子部分の素子構造に比べ周辺回路部分は非常に複雑な素子構造を取っている。従って、回路パターンが複雑になり、製造プロセス技術もより高度になり、コストが上昇する。また、当然に多層配線部分が増し、プロセス工程数の増加とＴＦＴの製造歩留りの低下が起こった。

【００１２】⑥周辺回路を構成するトランジスタは早い応答速度が要求されるため、通常は多結晶半導体を使用していた。そのため、半導体層を多結晶化するために、高温の処理を必要とし、高価な石英基板等を使用しなければならなかった。

【００１３】

【発明の構成】本発明は上記のような６つ問題を適度にバランスよく解決するものであり、コストが低く、製造歩留りの高い液晶表示装置に関するものである。

【００１４】すなわち、複数のゲート線、複数のソース（ドレイン）線および相補型構成の薄膜トランジスタを有する画素マトリクスが形成された第１の基板と前記第１の基板に対抗して配置された第２の基板と前記一対の基板間に保持された液晶組成物よりなる液晶表示装置で

あって、前記第１の基板上に形成されるＸまたはＹ方向のマトリクス配線に接続されている周辺回路のうちの少なくとも一部の周辺回路を前記画素に接続されたアクティブ素子と同様の相補型構成として、同一のプロセスで形成された薄膜トランジスタとし、残りの周辺回路は半導体チップで構成されているものであります。

【００１５】また、ＴＦＴ化しない残りの周辺回路としてのＩＣと基板との接続はＩＣチップを直接基板上に設けて、各接続端子と接続するＣＯＧ法やＩＣチップを１個毎にフレキシブルな有機樹脂基板上に設け、その樹脂基板とディスプレイ基板とを接続しするＴＡＢ法により、実現できる。

【００１６】すなわち、本発明は液晶表示装置の周辺回路の全てをＴＦＴ化するのでなく、素子構造の簡単な部分のみ、または素子数の少ない機能部分のみ、または汎用のＩＣが入手しにくい回路部分のみ、さらにはＩＣのコストが高い部分のみをＴＦＴ化して、液晶表示装置の製造歩留りを向上させるとともに、製造コストを下げることを目的とするものであります。

【００１７】また、周辺回路の一部をＴＦＴ化することにより、従来では相当な数が必要であった外付けのＩＣの数を減らし、製造コストを下げるものであります。

【００１８】さらにまた、アクティブ素子と周辺回路を同じプロセスにて作成した相補型構成（ＣＴＦＴ）の薄膜トランジスタとしたので、画素駆動の能力が向上し、周辺回路に冗長性を与えることができ、余裕のある液晶表示装置の駆動を行うことができた。

【００１９】また、周辺回路全部をＴＦＴ化するとディスプレイ用の基板の寸法をＸ方向およびＹ方向の両方に大きくする必要があり表示装置全体の専有面積が大きくなるが、一部のみをＴＦＴ化するとほんの少しだけ基板を大きくするだけですみ、表示装置を使用するコンピューターや装置の外形寸法に容易にあわせることができかつ専有面積と専有容積の少ない表示装置を実現できる。

【００２０】周辺回路中の素子構造が複雑である部分、例えば、多層配線が必要な素子構造やアンプの機能を持たせた部分等をＴＦＴ化するのに高度な作製技術が必要になるが、一部をＴＦＴ化することで、技術的に難しい部分は従来のＩＣを使用し、簡単な素子構造あるいは単純な機能の部分をＴＦＴ化でき、低コストで高い歩留りで表示装置を実現できる。

【００２１】また、一部のみＴＦＴ化することで、周辺回路部分の薄膜トランジスタの数を相当減らすことができる、単純にＸ方向、Ｙ方向の周辺回路の機能が同じ場合はほぼその数は半数となる。このように、ＴＦＴ化する素子数を減らすことで、基板の製造歩留りを向上させることができ、かつ基板の面積、容積を減少できた表示装置を低コストで実現することが可能となった。

【００２２】さらに、ＴＦＴに使用される半導体層を従来から使用されている、多結晶またはアモルファス半導体ではなく、新しい概念のセミアモルファス半導体を使用することで、低温で作製ができ、しかも、キャリアの移動度の非常に大きい、応答速度の早いＴＦＴを実現することができる。

【００２３】このセミアモルファス半導体とは、ＬＰＣＶＤ法、スパッタ法あるいはＰＣＶＤ法等により膜形成の後に熱結晶化処理を施して得られるが、以下にはスパッタ法を例にとり説明をする。

【００２４】すなわちスパッタ法において単結晶のシリコン半導体をターゲットとし、水素とアルゴンとの混合気体でスパッタをすると、アルゴンの重い原子のスパッタ（衝撃）によりターゲットからは原子状のシリコンが離れ、被形成面を有する基板上に飛しょうするが、同時に数十～数十万個の原子が固まった塊がクラスタとしてターゲットから離れ、被形成面に飛しょうする。

【００２５】この飛しょう中は、水素がこのクラスタの外周辺の珪素の不対結合手と結合し、結合した状態で被形成面上に秩序性の比較的高い領域として作られる。すなわち、被膜形成面上には秩序性の高い、かつ周辺にＳｉ－Ｈ結合を有するクラスタと純粋のアモルファス珪素との混合物の状態を実現する。これを４５０℃～７００℃の非酸化性気体中での熱処理により、クラスタの外周辺のＳｉ－Ｈ結合は他のＳｉ－Ｈ結合と反応し、Ｓｉ－Ｓｉ結合を作る。

【００２６】この結合はお互い引っぱりあうと同時に、秩序性の高いクラスタはより高い秩序性の高い状態、すなわち結晶化に相を移そうとする。しかし、隣合ったクラスタ間は、互いに結合したＳｉ－Ｓｉがそれぞれのクラスタ間を引っぱりあう。その結果は、結晶は格子歪を持ちレーザラマンでの結晶ピークは単結晶の５２０ｃｍ$^{-1}$より低波数側にずれて測定される。

【００２７】また、このクラスタ間のＳｉ－Ｓｉ結合は互いのクラスタをアンカリング（連結）するため、各クラスタでのエネルギバンドはこのアンカリングの個所を経て互いに電気的に連結しあえる。そのため結晶粒界がキャリアのバリアとして働く多結晶シリコンとは根本的に異なり、キャリア移動度も１０～２００ｃｍ^2／ＶＳｅｃを得ることができる。

【００２８】つまり、かるる定義に基づくセミアモルファス半導体は見掛け上結晶性を持ちながらも、電気的には結晶粒界が実質的にない状態を予想できる。もちろん、アニール温度がシリコン半導体の場合の４５０℃～７００℃という中温アニールではなく、１０００℃またはそれ以上の結晶成長をともなう結晶化をさせる時はこの結晶成長により、膜中の酸素等が粒界に折出し、バリアを作ってしまう。これは、単結晶と同じ結晶と粒界のある材料（多結晶）である。

【００２９】また、この半導体におけるクラスタ間のアンカリングの程度をより大きくすると、よりキャリア移動度は大きくなる。このためにはこの膜中にある酸素量

を7×10^{19} cm^{-3}好ましくは1×10^{19} cm^{-3}以下にすると、さらに600℃よりも低い温度で結晶化ができるに加えて、高いキャリア移動度を得ることができる。

【0030】

【実施例1】本実施例では図1に示すようなm×nの回路構成の液晶表示装置を用いて説明を行う。すなわち図1のX方向の配線に接続された周辺回路部分のうちアナログスイッチアレー回路部分1のみを画素6に設けられたアクティブ素子と同様にTFT化5し、Y方向配線に接続された周辺回路部分もアナログスイッチアレー回路部分2のみをTFT化しその他の周辺回路部分はIC4で、COG法により基板に接続している。ここで、TFT化した周辺回路部分は画素に設けられたアクティブ素子と同様にCTFT（相補型構成）として形成してある。

【0031】この回路構成に対応する実際の電極等の配置構成を図2に示している。図2は説明を簡単にする為2×2に相当する部分のみ記載されている。

【0032】まず、本実施例で使用する液晶表示装置上のTFTの作製方法を図3を使用して説明する。図3（A）において、石英ガラス等の高価でない700℃以下、例えば約600℃の熱処理に耐え得るガラス50上にマグネトロンRF（高周波）スパッタ法を用いてブロッキング層51としての酸化珪素膜を1000～3000Åの厚さに作製する。プロセス条件は酸素100％雰囲気、成膜温度15℃、出力400～800W、圧力0．5Paとした。ターゲットに石英または単結晶シリコンを用いた成膜速度は30～100Å／分であった。

【0033】この上にシリコン膜をLPCVD（減圧気相）法、スパッタ法またはプラズマCVD法により形成した。減圧気相法で形成する場合、結晶化温度よりも100～200℃低い450～550℃、例えば530℃でジシラン（Si_2H_6）またはトリシラン（Si_3H_8）をCVD装置に供給して成膜した。反応炉内圧力は30～300Paとした。成膜速度は50～250Å／分であった。NTFTとPTFTとのスレッシュホールド電圧（Vth）に概略同一に制御するため、ホウ素をジボランを用いて1×10^{15}～1×10^{18} cm^{-3}の濃度として成膜中に添加してもよい。

【0034】スパッタ法で行う場合、スパッタ前の背圧を1×10^{-5} Pa以下とし、単結晶シリコンをターゲットとして、アルゴンに水素を20～80％混入した雰囲気で行った。例えばアルゴン20％、水素80％とした。成膜温度は150℃、周波数は13．56MHz、スパッタ出力は400～800W、圧力は0．5Paであった。

【0035】プラズマCVD法により珪素膜を作製する場合、温度は例えば300℃とし、モノシラン（SiH_4）またはジシラン（Si_2H_6）を用いた。これらをPCVD装置内に導入し、13．56MHzの高周波電力を加えて成膜した。

【0036】これらの方法によって形成された被膜は、酸素が5×10^{21} cm^{-3}以下であることが好ましい。この酸素濃度が高いと、結晶化させにくく、熱アニール温度を高くまたは熱アニール時間を長くしなければならない。また少なすぎると、バックライトによりオフ状態のリーク電流が増加してしまう。そのため4×10^{19}～4×10^{21} cm^{-3}の範囲とした。水素は4×10^{20} cm^{-3}であり、珪素4×10^{22} cm^{-3}として比較すると1原子％であった。また、ソース、ドレインに対してより結晶化を助長させるため、酸素濃度を7×10^{19} cm^{-3}以下、好ましくは1×10^{19} cm^{-3}以下とし、ピクセル構成するTFTのチャネル形成領域のみに酸素をイオン注入法により5×10^{20}～5×10^{21} cm^{-3}となるように添加してもよい。その時周辺回路を構成するTFTには光照射がなされないため、この酸素の混入をより少なくし、より大きいキャリア移動度を有せしめることは、高周波動作をさせるため有効である。

【0037】次に、アモルファス状態の珪素膜を500～5000Å、例えば1500Åの厚さに作製の後、450～700℃の温度にて12～70時間非酸化物雰囲気にて中温の加熱処理、例えば水素雰囲気下にて600℃の温度で保持した。珪素膜の下の基板表面にアモルファス構造の酸化珪素膜が形成されているため、この熱処理で特定の核が存在せず、全体が均一に加熱アニールされる。即ち、成膜時はアモルファス構造を有し、また水素は単に混入しているのみである。

【0038】アニールにより、珪素膜はアモルファス構造から秩序性の高い状態に移り、一部は結晶状態を呈する。特にシリコンの成膜後の状態で比較的秩序性の高い領域は特に結晶化をして結晶状態となろうとする。しかしこれらの領域間に存在する珪素により互いの結合がなされるため、珪素同志は互いにひっぱりあう。レーザラマン分光により測定すると単結晶の珪素のピーク522 cm^{-1}より低周波側にシフトしたピークが観察される。それの見掛け上の粒径は半値巾から計算すると、50～500Åとマイクロクリスタルのようになっているが、実際はこの結晶性の高い領域は多数あってクラスタ構造を有し、各クラスタ間は互いに珪素同志で結合（アンカリング）がされたセミアモルファス構造の被膜を形成させることができた。

【0039】結果として、被膜は実質的にグレインバウンダリ（以下GBという）がないといってもよい状態を呈する。キャリアは各クラスタ間をアンカリングされた個所を通じ互いに容易に移動し得るため、いわゆるGBの明確に存在する多結晶珪素よりも高いキャリア移動度となる。即ちホール移動度（μh）＝10～200 cm^2／VSec、電子移動度（μe）＝15～300cm

^{2}／VSecが得られる。

【0040】他方、上記の如き中温でのアニールではなく、900～1200℃の高温アニールにより被膜を多結晶化すると、核からの固相成長により被膜中の不純物の偏析がおきて、GBには酸素、炭素、窒素等の不純物が多くなり、結晶中の移動度は大きいが、GBでのバリア（障壁）を作ってそこでのキャリアの移動を阻害してしまう。結果として10cm^2／Vsec以上の移動度がなかなか得られないのが実情である。即ち、本実施例ではかくの如き理由により、セミアモルファスまたはセミクリスタル構造を有するシリコン半導体を用いている。

【0041】図3（A）において、珪素膜を第1のフォトマスク①にてフォトエッチングを施し、PTFT用の領域22（チャネル巾20μm）を図面の右側に、NTFT用の領域13を左側に作製した。

【0042】この上に酸化珪素膜をゲイト絶縁膜として500～2000Å例えば1000Åの厚さに形成した。これはブロッキング層としての酸化珪素膜の作製と同一条件とした。この成膜中に弗素を少量添加し、ナトリウムイオンの固定化をさせてもよい。

【0043】この後、この上側にリンが1～5×10^{21}cm^{-3}の濃度に入ったシリコン膜またはこのシリコン膜とその上にモリブデン（Mo）、タングステン（W），$MoSi_2$またはWSi_2との多層膜を形成した。これを第2のフォトマスク②にてパターニングして図3（B）を得た。PTFT用のゲイト電極55、NTFT用のゲイト電極56を形成した。例えばチャネル長10μm、ゲイト電極としてリンドープ珪素を0．2μm、その上にモリブデンを0．3μmの厚さに形成した。　図3（C）において、フォトレジスト57をフォトマスク③を用いて形成し、PTFT用のソース59ドレイン58に対し、ホウ素を1～5×10^{15}cm^{-2}のドーズ量でイオン注入法により添加した。　次に図3（D）の如く、フォトレジスト61をフォトマスク④を用いて形成した。NTFT用のソース64、ドレイン62としてリンを1～5×10^{15}cm^{-2}のドーズ量でイオン注入法により添加した。

【0044】これらはゲイト絶縁膜54を通じて行った。しかし図3（B）において、ゲイト電極55、56をマスクとしてシリコン膜上の酸化珪素を除去し、その後、ホウ素、リンを直接珪素膜中にイオン注入してもよい。

【0045】次に、600℃にて10～50時間再び加熱アニールを行った。PTFTのソース59、ドレイン58NTFTのソース64、ドレイン62を不純物を活性化してP^+、N^+として作製した。またゲイト電極55、56下にはチャネル形成領域60、63がセミアモルファス半導体として形成されている。

【0046】かくすると、セルフアライン方式でありながらも、700℃以上にすべての工程で温度を加えることがなくC／TFTを作ることができる。そのため、基板材料として、石英等の高価な基板を用いいなくてもよく、本発明の大画素の液晶表示装置にきわめて適したプロセスである。

【0047】本実施例では熱アニールは図3（A）、（D）で2回行った。しかし図3（A）のアニールは求める特性により省略し、双方を図3（D）のアニールにより兼ね製造時間の短縮を図ってもよい。図3（E）において、層間絶縁物65を前記したスパッタ法により酸化珪素膜の形成として行った。この酸化珪素膜の形成はLPCVD法、光CVD法、常圧CVD法を用いてもよい。例えば0．2～0．6μmの厚さに形成し、その後、フォトマスク⑤を用いて電極用の窓66を形成した。さらに、これら全体にアルミニウムをスパッタ法により形成し、リード71、72およびコンタクト67、68をフォトマスク⑥を用いて作製した後、表面を平坦化用有機樹脂69例えば透光性ポリイミド樹脂を塗布形成し、再度の電極穴あけをフォトマスク⑦にて行った。

【0048】図3（F）に示す如く2つのTFTを相補型構成とし、かつその出力端を液晶装置の一方の画素の電極を透明電極としてそれに連結するため、スパッタ法によりITO（インジューム・スズ酸化膜）を形成した。それをフォトマスク⑧によりエッチングし、電極70を構成させた。このITOは室温～150℃で成膜し、200～400℃の酸素または大気中のアニールにより成就した。かくの如くにしてPTFT22とNTFT13と透明導電膜の電極70とを同一ガラス基板50上に作製した。得られたTFTの電気的な特性はPTFTで移動度は20（cm^2／Vs）、Vthは－5．9（V）で、NTFTで移動度は40（cm^2／Vs）、Vthは5．0（V）であった。

【0049】この液晶表示装置の画素部分の電極等の配置を図2に示している。NTFT13を第1の走査線15とデータ線21との交差部に設け、第1の走査線15とデータ線14との交差部にも他の画素用のNTFTが同様に設けられている。一方PTFTは第2の走査線18とデータ線21との交差部に設けられている。また、隣接した他の第1の走査線16とデータ線21との交差部には、他の画素用のNTFTが設けられている。このようなC／TFTを用いたマトリクス構成を有せしめた。NTFT13は、ドレイン64の入力端のコンタクトを介し第1の走査線15に連結され、ゲイト56は多層配線形成がなされたデータ線21に連結されている。ソース62の出力端はコンタクトを介して画素の電極17に連結している。

【0050】他方、PTFT22はドレイン58の入力端がコンタクトを介して第2の走査線18に連結され、ゲイト55はデータ線21に、ソース59の出力端はコンタクトを介してNTFTと同様に画素電極17に連結

している。かくして一対の走査線１５、１８に挟まれた間（内側）に、透明導電膜よりなる画素２３とC／TFTとにより１つのピクセルを構成せしめた。かかる構造を左右、上下に繰り返すことにより、２×２のマトリクスをそれを拡大した６４０×４８０、１２８０×９６０といった大画素の液晶表示装置とすることができる。

【００５１】このようにスイッチング素子と同じプロセスで作製されたNTFT１３とPTFT２２とが設けられたCMOS構成となっている。

【００５２】上記のようにして、片方の基板を完成し、他方の基板と従来よりの方法で貼り合わせ、STN液晶を基板間に注入する。次に、残りの周辺回路として、IC４を使用する。このIC４はCOGにより基板のX方向の配線およびY方向の配線の各々と接続されている。このIC４には外部から電源、データの供給の為の接続リードが各々に接続されているだけで、基板の一辺全てに接続の為のFPCが張りつけられているようなことはなく、接続部分の数が相当減り信頼性が向上する。上記のようにして、本発明の液晶表示装置を完成した。

【００５３】本実施例においては、X方向側の周辺回路のうちアナログスイッチアレー部分１のみをY方向側の周辺回路のうちアナログスイッチアレー部分２のみをTFT化し、スイッチング素子と同じプロセスでC／TFT化し、残りの周辺回路部分をIC４で構成したが、特にこの構成に限定されることはなく、TFT化する際の歩留り、TFT化する際のプロセス技術上の問題等を考慮して、よりTFT化が簡単な部分のみをTFT化すればよい。

【００５４】本実施例では半導体膜として、セミアモルファス半導体を使用したので、その移動度は非単結晶半導体を使用したTFTに比べて１０倍以上の値が得られている。そのため、早い応答速度を必要とされる周辺の回路のTFTにも、十分使用でき、従来のように、周辺回路部分のTFTを特別に結晶化処理する必要もなくアクティブ素子と同じプロセスで作成することができた。

【００５５】また、液晶の画素に接続されたアクティブ素子として、C／TFT構成としたので、動作マージンが拡大し、画素の電位がふらつくことはなく一定の表示レベルを確保でき、また一方のTFTが不良でも特に目立った欠陥表示都ならない等の利点があった。

【００５６】

【実施例２】本実施例の液晶表示装置の概略外観図を図４に示す。基本的な回路等は実施例１と全く同じである。図４において、Y方向の配線に接続された周辺回路のうちIC４で構成されている部分は、COG法により、基板上に直接ICが形成されている。このIC４は基板の上下の部分に分けて設けられている。

【００５７】この場合IC４のパッド電極とY方向配線との接続にいて、ICを片側のみに形成した場合に比べてより間隔を狭くできる。その為より高精細な表示画素を設計できる特徴をもつ。さらに、基板上にICを設けたので、その容積は殆ど増すことがなく、より薄型の液晶表示装置を提供することができた。

【００５８】上記の実施例において、アクティブ素子のTFTはいずれもCMOS構成としたが、特にこの構成に限定されることはなく、NTFT、PTFTのみで構成してもよい、その場合は周辺回路の構成がより素子数が増すことになる。

【００５９】また、基板上にTFTを形成する位置をX方向またはY方向の配線と繋がっている一方側のみではなく、もう一方の側にもTFTを形成して、交互にTFTを接続し、TFTの密度を半分として、TFTの製造歩留りを向上させることを実現した。

【００６０】

【発明の効果】本発明により、液晶表示を外部の接続技術上の制限の為に高精細化できないことはなくなった。また、X方向の配線またはY方向の配線と外部の周辺回路との不要な接続を極力へらせることができたので、接続部分での信頼性が向上した。

【００６１】一部の周辺回路のみをTFT化するため、ディスプレイ基板自身の専有面積をへらすことができ、かつ必要とされる寸法形状に自由に基板の設計ができる。また、TFTの製造上の問題を回避して、製造歩留りの高い部分のみをTFT化できる。よって、製造コストを下げることができた。

【００６２】TFTに使用する半導体膜として、セミアモルファス半導体を使用したので、周辺回路用にも十分使用できる応答速度が得られ、アクティブ素子の作成プロセスのまま特別な処理をすることもなく、周辺回路用のTFTを同時に作成することができた。

【００６３】本発明は相補型のTFTをマトリクス化された各画素に連結することにより、①しきい値の明確化　②スイッチング速度の増加　③動作マージンの拡大　④不良TFTが一部にあってもその補償をある程度行うことができる。　⑤作製に必要なフォトマスク数はNTFTのみの従来例に比べて２回多くなるのみである。⑥キャリアの移動度がアモルファス珪素を用いた場合に比べ１０倍以上も大きいため、TFTの大きさを小さくでき、１つのピクセル内に２つのTFTをつけても開口率の減少をほとんど伴わない。　という多くの特長を有する。

【００６４】そのため、これまでのNTFTのみを用いるアクティブTFT液晶装置に比べて、数段の製造歩留まりと画面の鮮やかさを成就できるようになった。

【図面の簡単な説明】

【図１】本発明のm×nの回路構成の液晶表示装置を示す。

【図２】本発明の液晶表示装置の画素部分の配置の様子を示す。

【図３】本発明のTFTの作製工程の概略を示す。

【図4】本発明のその他の実施例を示す。

【符号の説明】

1、2・・・・・周辺回路

4・・・・・・・・・・・IC

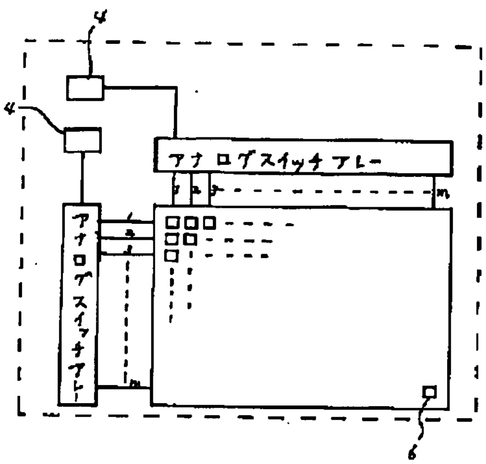
5・・・・・・・・・・・TFT化した周辺回路

6・・・・・・・・・・・画素

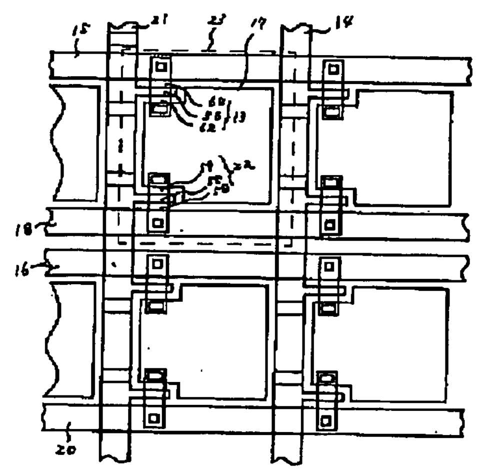
13・・・・・・・・・・NTFT

22・・・・・・・・・・PTFT

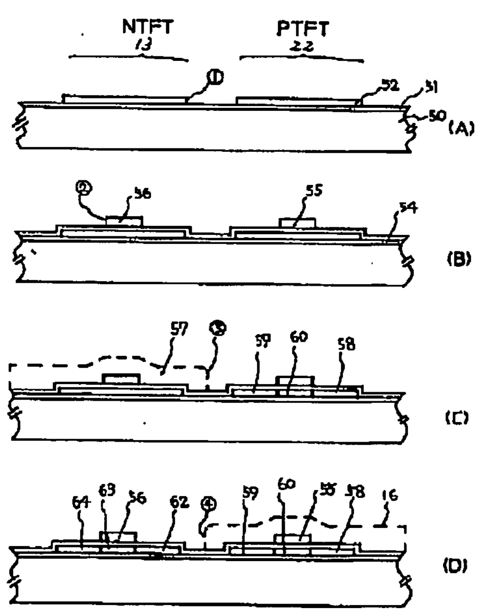
【図1】



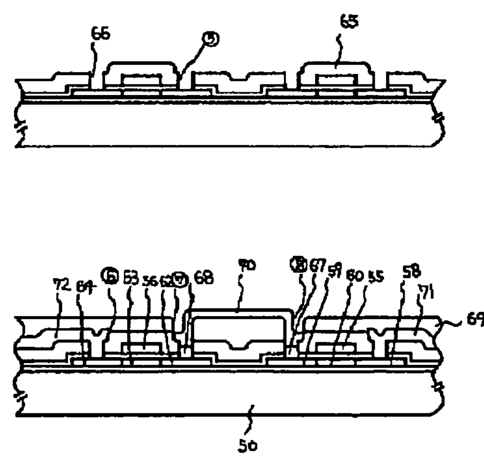
【図2】



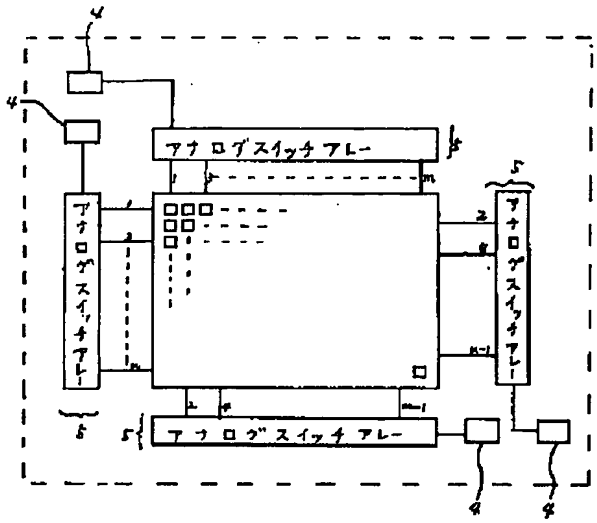
【図3】



【図3】

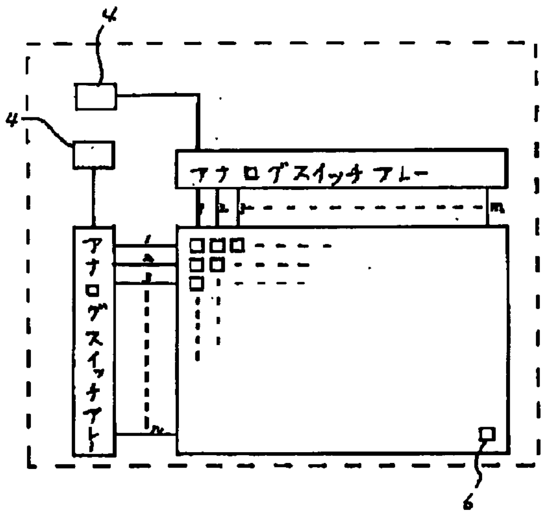


【図4】



【手続補正書】
【提出日】平成4年2月18日
【手続補正1】
【補正対象書類名】明細書
【補正対象項目名】図面の簡単な説明
【補正方法】変更
【補正内容】
【図面の簡単な説明】
【図1】本発明のm×nの回路構成の液晶表示装置を示す。
【図2】本発明の液晶表示装置の画素部分の配置の様子を示す。
【図3】本発明のＴＦＴの作製工程の概略を示す。
【図4】本発明のＴＦＴの作製工程の概略を示す。
【図5】本発明のその他の実施例を示す。
【符号の説明】
1、2・・・・・周辺回路
4・・・・・・・・・・・ＩＣ
5・・・・・・・・・・・ＴＦＴ化した周辺回路
6・・・・・・・・・・・画素
13・・・・・・・・・・ＮＴＦＴ
22・・・・・・・・・・ＰＴＦＴ
【手続補正2】
【補正対象書類名】図面
【補正対象項目名】全図
【補正方法】変更
【補正内容】

【図1】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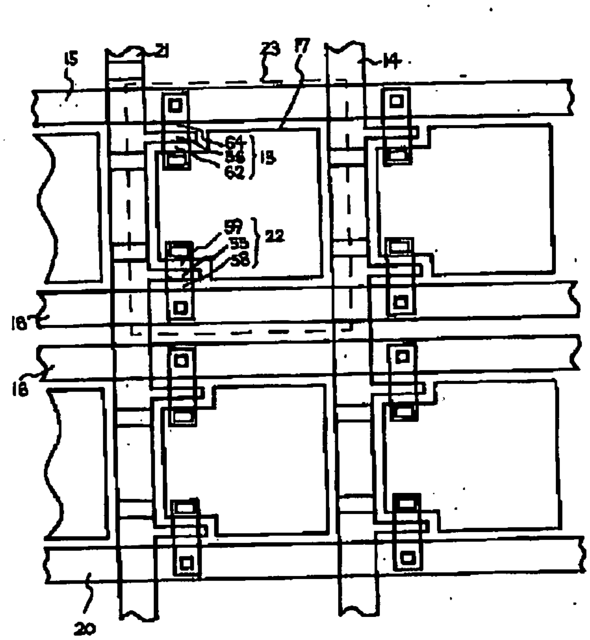
アナログスイッチアレー
4
4
6

【図2】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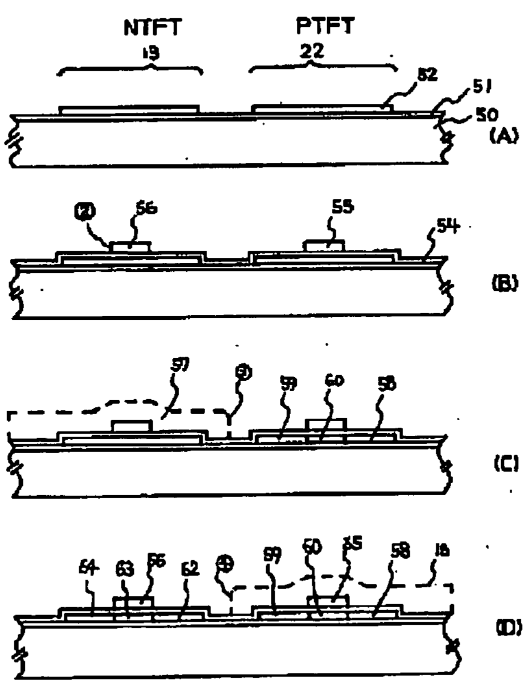
18
20

【図3】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PTFT
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52
51
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(A)
56
55
54
(B)
57
59
60
58
(C)
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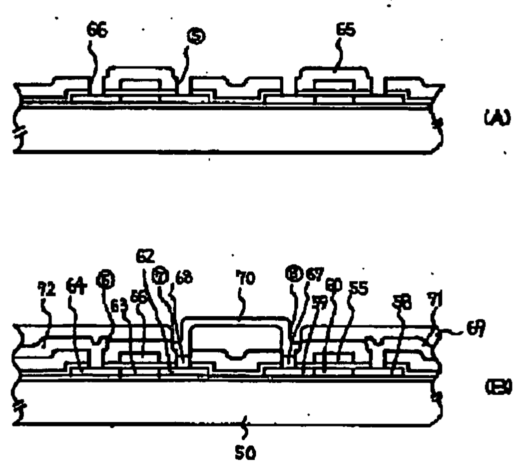
63
62
(D)

【図4】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(A)
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(B)
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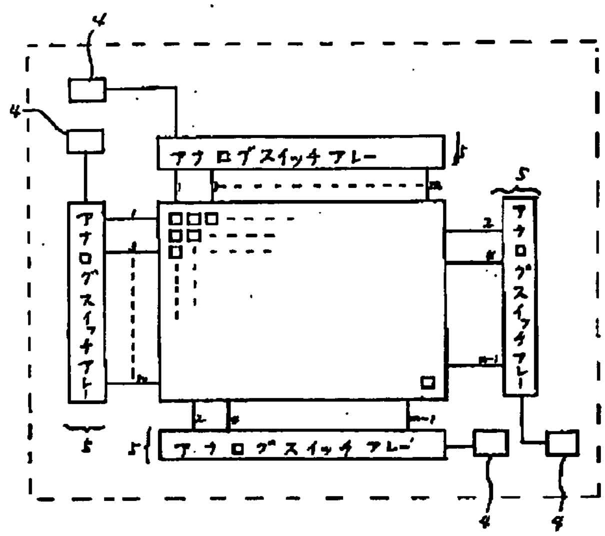
【図5】



US005453858A

United States Patent [19]

Yamazaki

[11] **Patent Number: 5,453,858**

[45] **Date of Patent: Sep. 26, 1995**

[54] **ELECTRO-OPTICAL DEVICE CONSTRUCTED WITH THIN FILM TRANSISTORS**

[75] Inventor: **Shunpei Yamazaki**, Tokyo, Japan

[73] Assignee: **Semiconductor Energy Laboratory Co., Ltd.**, Kanagawa, Japan

[21] Appl. No.: **384,593**

[22] Filed: **Feb. 3, 1995**

Related U.S. Application Data

[63] Continuation of Ser. No. 217,211, Mar. 24, 1994, abandoned, which is a continuation of Ser. No. 811,063, Dec. 20, 1991, abandoned.

[30] **Foreign Application Priority Data**

Dec. 25, 1990 [JP] Japan 2-418366
Dec. 25, 1990 [JP] Japan 2-418367

[51] **Int. Cl.^{6}** **G02F 1/1343**

[52] **U.S. Cl.** **359/59**; 359/85

[58] **Field of Search** 359/54, 55, 59, 359/58, 82, 84, 85; 340/719, 784; 257/52, 291, 296

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,470,060	9/1984	Yamazaki	359/58
4,838,654	6/1989	Hamaguchi et al.	359/59
5,151,689	9/1992	Kabuto et al.	359/59

FOREIGN PATENT DOCUMENTS

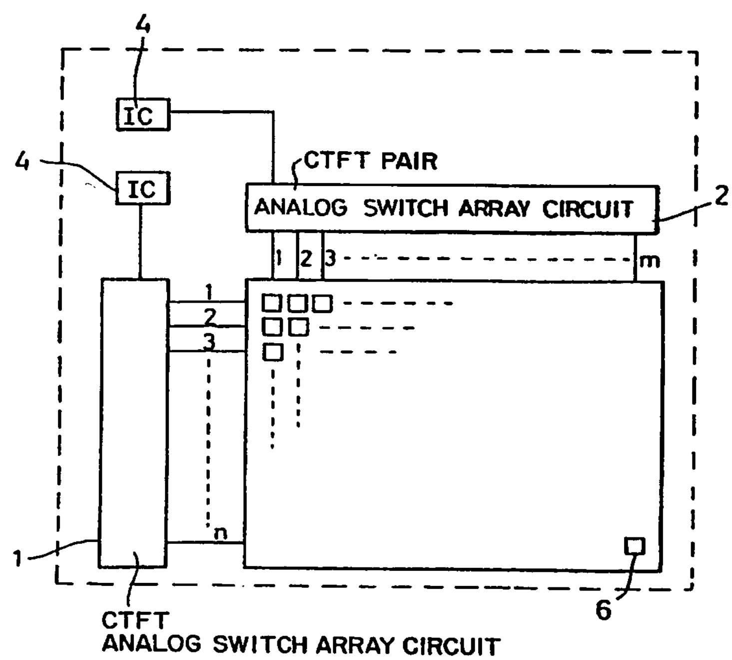
0144297	12/1978	Japan	359/59
0004021	1/1986	Japan	359/59

Primary Examiner—William L. Sikes
Assistant Examiner—Huy Mai
Attorney, Agent, or Firm—Sixbey, Friedman, Leedom & Ferguson; Gerald J. Ferguson, Jr.; Evan R. Smith

[57] **ABSTRACT**

An electro-optical device and a method for manufacturing the same are disclosed. The device comprises a pair of substrates and an electro-optical modulating layer (e.g. a liquid crystal layer having sandwiched therebetween, said pair of substrates consisting of a first substrate having provided thereon a plurality of gate wires, a plurality of source (drain) wires, and a pixel matrix comprising thin film transistors, and a second substrate facing the first substrate, wherein, among the peripheral circuits having established on the first substrate and being connected to the matrix wirings for the X direction and the Y direction, only a part of said peripheral circuits is constructed from thin film semiconductor devices fabricated by the same process utilized for an active device, and the rest of the peripheral circuits is constructed from semiconductor chips. The liquid crystal display device according to the present invention is characterized by that the peripheral circuits are not wholly fabricated into thin film transistors, but only those portions having a simple device structure, or those composed of a small number of devices, or those comprising an IC not easily available commercially, or those comprising an expensive integrated circuit, are fabricated by thin film transistors. According to the present invention, an electro-optical device is provided at an increased production yield with a reduced production cost.

15 Claims, 9 Drawing Sheets



US005514879A

United States Patent [19]

Yamazaki

[11] Patent Number: 5,514,879

[45] Date of Patent: May 7, 1996

[54] GATE INSULATED FIELD EFFECT TRANSISTORS AND METHOD OF MANUFACTURING THE SAME

[75] Inventor: Shunpei Yamazaki, Tokyo, Japan

[73] Assignee: Semiconductor Energy Laboratory Co., Ltd., Kanagawa, Japan

[21] Appl. No.: 479,392

[22] Filed: Jun. 7, 1995

Related U.S. Application Data

[62] Division of Ser. No. 293,201, Aug. 19, 1994, which is a continuation of Ser. No. 967,564, Oct. 28, 1992, abandoned, which is a continuation of Ser. No. 673,821, Mar. 22, 1991, abandoned.

[30] **Foreign Application Priority Data**

Nov. 20, 1990	[JP]	Japan	2-316598
Nov. 26, 1990	[JP]	Japan	2-323696

[51] Int. Cl.^{6} H01L 29/04

[52] U.S. Cl. 257/65; 257/66; 257/72

[58] Field of Search 257/57, 58, 59, 257/61, 66, 72, 435, 607, 65

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,818,077	4/1989	Ohwada et al.	359/59
5,082,351	1/1992	Fergason	359/51
5,132,820	7/1992	Someya et al.	359/54
5,313,076	5/1994	Yamazaki et al.	257/65
5,383,041	1/1995	Yamazaki et al.	359/59

FOREIGN PATENT DOCUMENTS

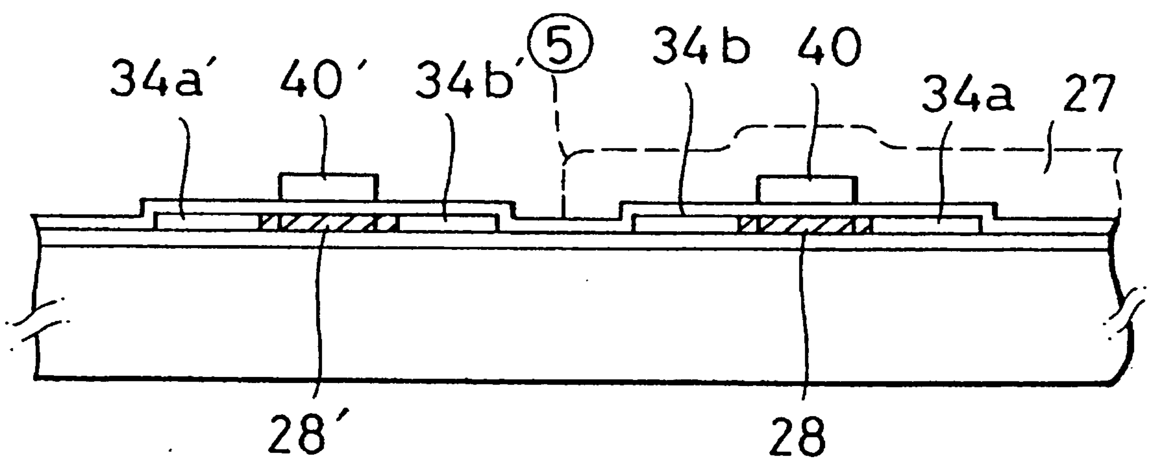
0144297	12/1978	Japan	359/59
63-096636	4/1988	Japan	359/59
1068724	3/1989	Japan	340/784
1107237	4/1989	Japan	340/784

Primary Examiner—Sara W. Crane
Assistant Examiner—Courtney A. Bowers
Attorney, Agent, or Firm—Sixbey, Friedman, Leedom & Ferguson; Gerald J. Ferguson, Jr.; Eric J. Robinson

[57] **ABSTRACT**

A thin film field effect transistors and manufacturing method for the same are described. The channel region of the transistor is spoiled by an impurity such as oxygen, carbon, nitrogen. The photosensitivity of the channel region is reduced by the spoiling impurity and therefore the transistor is endowed with immunity to illumination incident thereupon which would otherwise impair the normal operation of the transistor. The spoiling impurity is not introduced into transistors which are located in order not to receive light rays.

8 Claims, 15 Drawing Sheets



US005614732A

United States Patent [19]

Yamazaki

[11] Patent Number: 5,614,732

[45] Date of Patent: *Mar. 25, 1997

[54] **GATE INSULATED FIELD EFFECT TRANSISTORS AND METHOD OF MANUFACTURING THE SAME**

[75] Inventor: **Shunpei Yamazaki**, Tokyo, Japan

[73] Assignee: **Semiconductor Energy Laboratory Co., Ltd.**, Atsugi, Japan

[*] Notice: The term of this patent shall not extend beyond the expiration date of Pat. No. 5,514,879.

[21] Appl. No.: **293,201**

[22] Filed: **Aug. 19, 1994**

Related U.S. Application Data

[63] Continuation of Ser. No. 967,564, Oct. 28, 1992, abandoned, which is a continuation of Ser. No. 673,821, Mar. 22, 1991, abandoned.

[30] **Foreign Application Priority Data**

Nov. 20, 1990	[JP]	Japan	2-316598
Nov. 26, 1990	[JP]	Japan	2-323696

[51] **Int. Cl.**^{6} **H01L 29/76**; H01L 29/04

[52] **U.S. Cl.** **257/66**; 257/57; 257/58; 257/59; 257/72

[58] **Field of Search** 357/23.7, 4; 257/66, 257/57, 58, 59, 72, 61; 359/59

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,621,276	11/1986	Malhi	257/66
4,659,392	4/1987	Vasudev .	
4,755,865	7/1988	Wilson et al.	257/66
4,766,477	8/1988	Nakagawa et al. .	
4,772,927	9/1988	Saito et al. .	
4,818,077	4/1989	Ohwada et al.	359/59
4,849,797	7/1989	Ukai et al.	257/57
4,864,376	9/1989	Aoki et al.	257/61
5,037,766	8/1991	Wang .	
5,057,889	10/1991	Yamada et al.	257/61
5,082,351	1/1992	Fergason	359/51
5,132,820	7/1992	Someya et al.	359/54
5,270,567	12/1993	Mori et al.	257/66
5,383,041	1/1995	Yamazaki et al.	359/59

FOREIGN PATENT DOCUMENTS

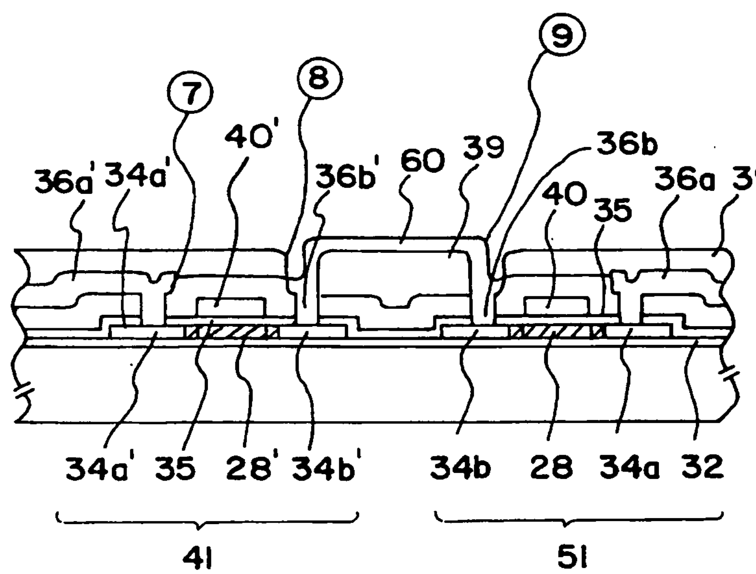
0144297	of 1978	Japan	359/59
53-144297	12/1978	Japan .	
0096636	of 1988	Japan	359/59
63-096636	4/1988	Japan .	
63-219172	9/1988	Japan	257/57
0068724	of 1989	Japan	340/784
0107237	of 1989	Japan	340/784
1068724	3/1989	Japan .	
1107237	4/1989	Japan .	
262077	3/1990	Japan	257/72

Primary Examiner—Mahshid D. Saadat
Assistant Examiner—Jhihan B. Clark
Attorney, Agent, or Firm—Sixbey, Friedman, Leedom & Ferguson, P.C.; Gerald J. Ferguson, Jr.; Eric J. Robinson

[57] **ABSTRACT**

A thin film field effect transistors and manufacturing method for the same are described. The channel region of the transistor is spoiled by an impurity such as oxygen, carbon, nitrogen. The photosensitivity of the channel region is reduced by the spoiling impurity and therefore the transistor is endowed with immunity to illumination incident thereupon which would otherwise impair the normal operation of the transistor. The spoiling impurity is not introduced into transistors which are located in order not to receive light rays.

41 Claims, 15 Drawing Sheets



US005701167A

United States Patent [19]

Yamazaki

[11] Patent Number: 5,701,167

[45] Date of Patent: Dec. 23, 1997

[54] **LCD HAVING A PERIPHERAL CIRCUIT WITH TFTS HAVING THE SAME STRUCTURE AS TFTS IN THE DISPLAY REGION**

[75] Inventor: **Shunpei Yamazaki**, Tokyo, Japan

[73] Assignee: **Semiconductor Energy Laboratory Co., Ltd.**, Kanagawa-ken, Japan

[21] Appl. No.: **712,574**

[22] Filed: **Sep. 13, 1996**

Related U.S. Application Data

[60] Continuation of Ser. No. 500,241, Jul. 10, 1995, abandoned, which is a division of Ser. No. 384,593, Feb. 3, 1995, Pat. No. 5,453,858, which is a continuation of Ser. No. 217,211, Mar. 24, 1994, abandoned, which is a continuation of Ser. No. 811,063, Dec. 20, 1991, abandoned.

[30] **Foreign Application Priority Data**

Dec. 25, 1990 [JP] Japan 2-418366
Dec. 25, 1990 [JP] Japan 2-418367

[51] **Int. Cl.**^{6} **G02F 1/136**; G02F 1/1345

[52] **U.S. Cl.** **349/42**; 349/149

[58] **Field of Search** 359/59, 58, 88; 257/59; 349/41, 42, 151, 149

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,470,060	9/1984	Yamazaki	359/58
4,838,654	6/1989	Hamaguchi et al.	359/59
5,151,689	9/1992	Kabuto et al.	359/59
5,247,191	9/1993	Yamazaki et al.	257/72
5,250,931	10/1993	Misawa et al.	359/59

FOREIGN PATENT DOCUMENTS

0144297	10/1978	Japan .
58-27364	2/1983	Japan .
0004021	7/1986	Japan .
63-96636	4/1988	Japan .
1128534	5/1989	Japan .
1289917	11/1989	Japan .
2223912	9/1990	Japan .
2251992	10/1990	Japan .

OTHER PUBLICATIONS

"An Active Matrix LCD with Integrated Driver Circuits Using a Si TFTs" M. Aklyama et al., Japan Display, pp. 212–215.

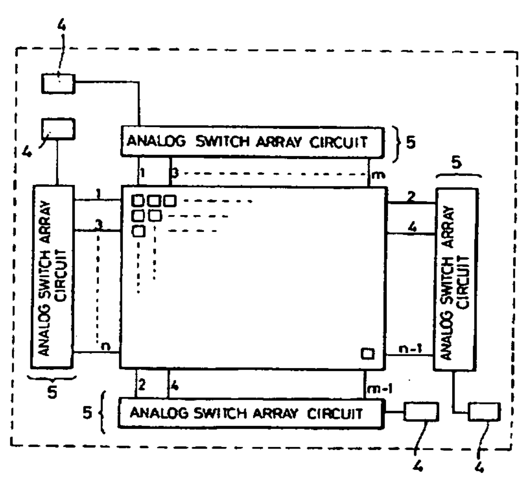
"Color Liquid Crystal Display", Shunsuke Kobayashi, Dec. 14, 1990, pp. 162–166.

Primary Examiner—William L. Sikes
Assistant Examiner—Toan Ton
Attorney, Agent, or Firm—Sixbey, Friedman, Leedom & Ferguson, P.C.; Gerald J. Ferguson, Jr.; Eric J. Robinson

[57] **ABSTRACT**

An electro-optical device and a method for manufacturing the same are disclosed. The device comprises a pair of substrates and an electro-optical modulating layer (e.g. a liquid crystal layer having sandwiched therebetween, said pair of substrates consisting of a first substrate having provided thereon a plurality of gate wires, a plurality of source (drain) wires, and a pixel matrix comprising thin film transistors, and a second substrate facing the first substrate, wherein, among the peripheral circuits having established on the first substrate and being connected to the matrix wirings for the X direction and the Y direction, only a part of said peripheral circuits is constructed from thin film semiconductor devices fabricated by the same process utilized for an active device, and the rest of the peripheral circuits is constructed from semiconductor chips. The liquid crystal display device according to the present invention is characterized by that the peripheral circuits are not wholly fabricated into thin film transistors, but only those portions having a simple device structure, or those composed of a small number of devices, or those comprising an IC not easily available commercially, or those comprising an expensive integrated circuit, are fabricated by thin film transistors. According to the present invention, an electro-optical device is provided at an increased production yield with a reduced production cost.

6 Claims, 9 Drawing Sheets



US005849601A

United States Patent [19]

Yamazaki

[11] **Patent Number: 5,849,601**

[45] **Date of Patent: Dec. 15, 1998**

[54] **ELECTRO-OPTICAL DEVICE AND METHOD FOR MANUFACTURING THE SAME**

[75] Inventor: **Shunpei Yamazaki**, Tokyo, Japan

[73] Assignee: **Semiconductor Energy Laboratory Co., Ltd.**, Atsugi, Japan

[21] Appl. No.: **231,644**

[22] Filed: **Apr. 22, 1994**

Related U.S. Application Data

[62] Division of Ser. No. 217,211, Mar. 24, 1994, abandoned, which is a continuation of Ser. No. 811,063, Dec. 20, 1991, abandoned.

[30] **Foreign Application Priority Data**

Dec. 25, 1990 [JP] Japan 2-418366
Dec. 25, 1990 [JP] Japan 2-418367

[51] **Int. Cl.**[6] **H01L 21/20**

[52] **U.S. Cl.** **437/101**; 437/173; 142/DIG. 1

[58] **Field of Search** 437/101, 173; 148/DIG. 1

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,363,828	12/1982	Brodsky et al.	427/39
4,438,654	3/1984	Hamaguchi et al.	359/59

(List continued on next page.)

FOREIGN PATENT DOCUMENTS

55-011329	1/1980	Japan .
55-029154	3/1980	Japan .
55-050663	4/1980	Japan .
55-050664	4/1980	Japan .
58-092217	6/1983	Japan .
58-155773	9/1983	Japan .
58-155774	9/1983	Japan .
58-161380	9/1983	Japan .
59-035423	2/1984	Japan .
59-035488	2/1984	Japan .
59-072128	4/1984	Japan .
59-072182	4/1984	Japan .
59-115574	7/1984	Japan .
60-245172	12/1985	Japan .
60-245173	12/1985	Japan .
60-245174	12/1985	Japan .
268064	10/1989	Japan .
32090924	12/1991	Japan .

OTHER PUBLICATIONS

VLSI Technology, Edited by S.M. Sze, McGraw–Hill Book Company, "Chapter 6 Dielectric and Polysilicon Film Deposition" A.C. Adams, pp. 233–235.

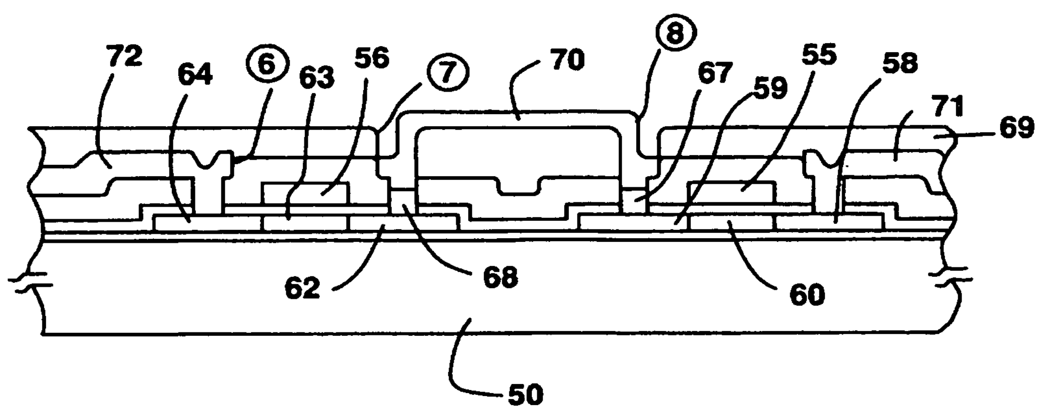
(List continued on next page.)

Primary Examiner—Robert Kunemund
Attorney, Agent, or Firm—Sixbey, Friedman, Leedom & Ferguson, P.C.; Gerald J. Ferguson, Jr.; Eric J. Robinson

[57] **ABSTRACT**

An electro-optical device and a method for manufacturing the same are disclosed. The device comprises a pair of substrates and an electro-optical modulating layer (e.g. a liquid crystal layer having sandwiched therebetween, said pair of substrates consisting of a first substrate having provided thereon a plurality of gate wires, a plurality of source (drain) wires, and a pixel matrix comprising thin film transistors, and a second substrate facing the first substrate, wherein, among the peripheral circuits having established on the first substrate and being connected to the matrix wirings for the X direction and the Y direction, only a part of said peripheral circuits is constructed from thin film semiconductor devices fabricated by the same process utilized for an active device, and the rest of the peripheral circuits is constructed from semiconductor chips. The liquid crystal display device according to the present invention is characterized by that the peripheral circuits are not wholly fabricated into thin film transistors, but only those portions having a simple device structure, or those composed of a small number of devices, or those comprising an IC not easily available commercially, or those comprising an expensive integrated circuit, are fabricated by thin film transistors. According to the present invention, an electro-optical device is provided at an increased production yield with a reduced production cost.

18 Claims, 10 Drawing Sheets



US005859445A

United States Patent [19]

Yamazaki

[11] **Patent Number: 5,859,445**

[45] **Date of Patent: *Jan. 12, 1999**

[54] **ELECTRO-OPTICAL DEVICE INCLUDING THIN FILM TRANSISTORS HAVING SPOILING IMPURITIES ADDED THERETO**

[75] Inventor: **Shunpei Yamazaki**, Tokyo, Japan

[73] Assignee: **Semiconductor Energy Laboratory Co., Ltd.**, Kanagawa-ken, Japan

[*] Notice: The term of this patent shall not extend beyond the expiration date of Pat. No. 5,614,732.

[21] Appl. No.: **799,369**

[22] Filed: **Feb. 14, 1997**

Related U.S. Application Data

[62] Division of Ser. No. 293,201, Aug. 19, 1994, Pat. No. 5,614,732, which is a continuation of Ser. No. 967,564, Oct. 28, 1992, abandoned, which is a continuation of Ser. No. 673,821, Mar. 22, 1991, abandoned.

[30] **Foreign Application Priority Data**

Nov. 20, 1990	[JP]	Japan	2-316598
Nov. 26, 1990	[JP]	Japan	2-323696

[51] **Int. Cl.**^{6} **H01L 29/04**; H01L 29/76; H01L 31/036

[52] **U.S. Cl.** **257/66**; 257/57; 257/58; 257/59; 257/61; 257/72

[58] **Field of Search** 257/57, 58, 59, 257/61, 72, 66; 359/59

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,363,828	12/1982	Brodsky et al.	427/574
4,460,670	7/1984	Ogawa et al.	430/57
4,470,060	9/1984	Yamazaki	257/59

(List continued on next page.)

FOREIGN PATENT DOCUMENTS

0144297	12/1978	Japan	359/59
55-011329	1/1980	Japan .	
55-029154	3/1980	Japan .	
55-050663	4/1980	Japan .	
55-050664	4/1980	Japan .	
55-82458	6/1980	Japan .	
58-27364	2/1983	Japan .	
58-092217	6/1983	Japan .	
58-155773	9/1983	Japan .	
58-155774	9/1983	Japan .	
58-161380	9/1983	Japan .	
59-035423	2/1984	Japan .	
59-035488	2/1984	Japan .	

(List continued on next page.)

OTHER PUBLICATIONS

VLSI Technology, Edited by S.M. Sze, McGraw–Hill Book Company, "Chapter 6 Dielectric and Polysilicon Film Deposition" A.C. Adams, pp. 233–235.

Scheid, et al., "Super Large Grain Polycrystalline Silicon Obtained From Pyrolysis of Si_2H_6 and Annealing" Jap. J. Appl. Phys. vol. 29, No. 11, Nov. 1990, pp. L 2105–2107.

Blum et al. "Low Pressure CVD Process for Micro and Polycrystalline Silicon" IBM Technical Disclosure Bulletin vol. 26, No. 3A, Aug. 1983, pp. 921–922.

Madsen et al. "In Situ Doping of Silicon Films Prepared by Low Pressure Chemical Vapor Deposition Using Disilane and Phosphine" J. Electrochem. Soc., col. 137, No. 7, Jul. 1990, pp. 2246–2251.

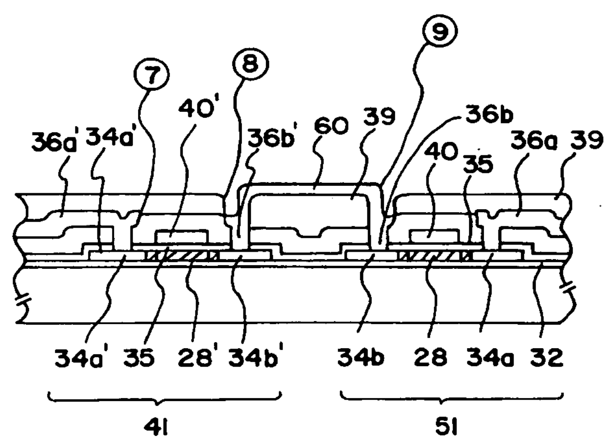
(List continued on next page.)

Primary Examiner—Mahshid Saadat
Assistant Examiner—Jhihan B. Clark
Attorney, Agent, or Firm—Sixbey, Friedman, Leedom & Ferguson, PC; Gerald J. Ferguson, Jr.; Eric J. Robinson

[57] **ABSTRACT**

An electro-optical device having a plurality of pixel electrodes, each with at least one thin film transistor. The channel region of the transistor is spoiled by an impurity such as oxygen, carbon, or nitrogen. The photosensitivity of the channel region is reduced by the spoiling impurity and therefore the transistor includes immunity to illumination incident thereupon, which would otherwise impair the normal operation of the transistor. The spoiling impurity is not introduced into transistors that are located such that they do not receive light rays.

49 Claims, 15 Drawing Sheets



US006023075A

United States Patent [19]

Yamazaki

[11] **Patent Number: 6,023,075**

[45] **Date of Patent: Feb. 8, 2000**

[54] **ELECTRO-OPTICAL DEVICE AND METHOD FOR MANUFACTURING THE SAME**

[75] Inventor: **Shunpei Yamazaki**, Tokyo, Japan

[73] Assignee: **Semiconductor Energy Laboratory Co., Ltd.**, Kanagawa-ken, Japan

[21] Appl. No.: **08/962,601**

[22] Filed: **Oct. 31, 1997**

Related U.S. Application Data

[62] Division of application No. 08/231,644, Apr. 22, 1994, Pat. No. 5,849,601, which is a division of application No. 08/217,211, Mar. 24, 1994, abandoned, which is a continuation of application No. 07/811,063, Dec. 20, 1991, abandoned, which is a continuation-in-part of application No. 08/293,201, Aug. 19, 1994, Pat. No. 5,614,732, which is a continuation of application No. 07/967,564, Oct. 28, 1992, abandoned, which is a continuation of application No. 07/673,821, Mar. 22, 1991, abandoned.

[30] **Foreign Application Priority Data**

Dec. 25, 1990	[JP]	Japan	2-418366
Dec. 25, 1990	[JP]	Japan	2-418367

[51] **Int. Cl.**^{7} **H01L 27/13**; H01L 29/786

[52] **U.S. Cl.** **257/72**; 257/59; 257/67; 257/351

[58] **Field of Search** 257/59, 72, 351, 257/67

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,068,020	1/1978	Reuschel .
4,103,297	7/1978	McGreivy et al. .
4,239,346	12/1980	Lloyd .
4,363,828	12/1982	Brodsky et al. .
4,365,013	12/1982	Ishioka et al. .

(List continued on next page.)

FOREIGN PATENT DOCUMENTS

0 161 555	11/1985	European Pat. Off. .
0321073	6/1989	European Pat. Off. .
49-77537	7/1974	Japan .
0144297	12/1978	Japan .
55-011329	1/1980	Japan .

(List continued on next page.)

OTHER PUBLICATIONS

VLSI Technology, Edited by S.M. Sze, McGraw-Hill Book Company, "Chapter 6 Dielectric and Polysilicon Film Deposition" A.C. Adams, pp. 233–235.

(List continued on next page.)

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[57] **ABSTRACT**

An electro-optical device and a method for manufacturing the same are disclosed. The device comprises a pair of substrates and an electro-optical modulating layer (e.g. a liquid crystal layer having sandwiched therebetween, said pair of substrates consisting of a first substrate having provided thereon a plurality of gate wires, a plurality of source (drain) wires, and a pixel matrix comprising thin film transistors, and a second substrate facing the first substrate, wherein, among the peripheral circuits having established on the first substrate and being connected to the matrix wirings for the X direction and the Y direction, only a part of said peripheral circuits is constructed from thin film semiconductor devices fabricated by the same process utilized for an active device, and the rest of the peripheral circuits is constructed from semiconductor chips. The liquid crystal display device according to the present invention is characterized by that the peripheral circuits are not wholly fabricated into thin film transistors, but only those portions having a simple device structure, or those composed of a small number of devices, or those comprising an IC not easily available commercially, or those comprising an expensive integrated circuit, are fabricated by thin film transistors. According to the present invention, an electro-optical device is provided at an increased production yield with a reduced production cost.

46 Claims, 7 Drawing Sheets